

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABILITY OF VLSI DESIGNS						
<p>Application Number :</p> <p>Confirmation Number:</p> <p>First Named Applicant: Robert Allen</p> <p>Attorney Docket Number: BUR920030092US1</p> <p>Art Unit:</p> <p>Examiner:</p> <p>Search string: (4831725 or 5459690 or 5796274 or 5798937 or 6026224 or 6189132 or 6484301 or 6556658).pn</p>							
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
<i>MW</i>	1	4831725	1989-05-23	Dunham et al.			
<i>MW</i>	2	5459690	1995-10-17	Rieger et al.			
<i>MW</i>	3	5796274	1998-08-18	Willis et al.			
<i>MW</i>	4	5798937	1998-08-25	Bracha et al.			
<i>MW</i>	5	6026224	2000-02-15	Darden et al.			
<i>MW</i>	6	6189132	2001-02-13	Heng et al.			
<i>MW</i>	7	6484301	2002-11-19	Burden			
<i>MW</i>	8	6556658	2003-04-29	Brennan			
Signature							
Examiner Name				Date			
<i>MWileczewski</i>				<i>3/2005</i>			

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